REMARKS

This communication responds to the Office Action dated April 6, 2009.

No claims are amended, canceled, or added by this Response. Claims 1-26 remain pending in this application.

§ 112 Rejection of the Claims

Claim 1 was rejected under 35 U.S.C. § 112, first paragraph, as lacking adequate description or enablement. In particular, the Office Action states that the specification is silent regarding the elements

> each conductive layer is electrically connected to a constant voltage to form a constant voltage plane, wherein the multi-layer circuit board is arranged substantially parallel to the hermetic seal and normal to the I/O conductors to provide electrical shielding, and wherein one I/O conductor provides an electrical connection to the constant voltage plane,

and again asserts that these elements are nowhere described or disclosed in the specification.

Applicant respectfully traverses the rejection and respectfully submits that the elements are indeed described in the specification in such a way as to reasonably convey to one of ordinary skill in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention.

Regarding *each conductive layer is electrically connected to a constant voltage to form a constant voltage plane:*

As shown in FIG. 5A and as described on page 7 line 8 of the application, layer one 510 is a ground layer (a first conductive layer). As shown in FIG. 5C and as described on page 7 line 19, layer three 530 is a ground layer (a second conductive layer). Thus, the specification shows a first and second conductive layer, each conductive layer connected to a constant voltage (e.g., ground) to form a constant voltage plane.

Regarding *wherein one I/O conductor provides an electrical connection to the constant voltage plane:*

As shown in FIG. 5A and as described on page 7 lines 9-12, the layer 510 shows that when holes 430 are formed in the substrate 300, the metal layout isolates nine of the pin

locations 511 from the ground layer while one pin location 512 will be connected to ground. Thus, the specification shows that one I/O conductor provides an electrical connection to the constant voltage plane.

Regarding *wherein the multi-layer circuit board is arranged substantially parallel to the hermetic seal and normal to the I/O conductors to provide electrical shielding:*

FIG. 2A shows a filtered feedthrough assembly. FIG. 2A shows and the specification describes on page 4 lines 20-21 describe that a hermetic seal is formed by a hermetic layer 210 surrounded by a metal plate. FIG. 2A shows and page 5 lines 16-17 describe that discrete capacitors are formed on a printed circuit substrate [250]. It can be seen in FIG. 2A that the printed circuit substrate is substantially parallel to the hermetic layer 210. Page 6 lines 18-19 describe using a multi-layer circuit board for the printed circuit substrate 300. Thus, the specification shows that the multi-layer circuit board is arranged substantially parallel to the hermetic seal. FIG. 2A also shows I/O conductors that are normal to the printed circuit substrate or multi-layer circuit board.

The specification describes on page 7 lines 19-21 that layer three [of the multi-layer circuit board] is a ground layer and layer three is the bottom-most layer and faces the hermetic seal when the feedthrough assembly 200 is formed. One of ordinary skill in the art would recognize, upon reading the specification, that the ground layer would provide electrical shielding. Thus, the specification shows the multi-layer circuit board is arranged substantially parallel to the hermetic seal and normal to the I/O conductors to provide electrical shielding.

Therefore, the elements are indeed described in the specification in such a way as to reasonably convey to one of ordinary skill in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention. Consequently, withdrawal of the rejection and allowance of claim 1 is respectfully requested.

§ *103 Rejection of the Claims*

1. Claims 1-6, 8-12, 15-18 and 23-26 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Hittman et al. (U.S. Patent No. 5,896,267, hereinafter "Hittman") in view of Truex et al. (U.S. Patent No. 5,683,435, hereinafter "Truex"). Applicant respectfully traverses the rejection.

Applicant respectfully submits that claim 1 is allowable over the proposed combination of Hittman and Truex because the cited portions of the references do not teach or suggest all of the subject matter in the claims. For example, Applicant is unable to find in the cited portions of these references, among other things,

> a printed circuit interconnect substrate residing on the hermetic side of the hermetic seal, wherein the printed circuit interconnect substrate includes a multi-layer circuit board comprising a buried signal layer between first and second conductive layers, wherein each conductive layer is electrically connected to a constant voltage to form a constant voltage plane, and wherein the multi-layer circuit board is arranged substantially parallel to the hermetic seal and normal to the I/O conductors,

as presently recited in claim 1. As stated in the present Patent Application, this allows the filters to be placed as close as possible to the hermetic seal.[1]

The Office Action concedes that Hittman does not specifically disclose a printed circuit interconnect substrate that includes a multi-layer circuit board comprising a buried signal layer between first and second conductive layers wherein each conductive layer is electrically connected to a constant voltage to form a constant voltage plane, but states that Truex teaches a feedthrough assembly (10) ... comprising a multilayer circuit board (34) having a signal layer between first and second conductive layers , wherein each conductive layer is electrically connected to a constant voltage to form a constant voltage plane. [2]

However, in contrast to the present subject matter, Truex refers to a multilayered structure 34 that extends through and is hermetically sealed to the interior of the weld ring 32 at an intermediate portion 30.[3] Thus, Truex does not teach or suggest "a printed circuit interconnect substrate residing on the hermetic side of the hermetic seal," but instead resides on both sides of the hermetic seal.

Additionally, the multilayered structure 34 of Truex is arranged parallel to printed conductors 56 and normal to the hermetic seal.[4] Thus, Truex with Hittman does not teach or suggest "wherein the multi-layer circuit board is arranged substantially parallel to the hermetic seal and normal to the I/O conductors," as recited in claim 1.

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[1] Patent Application, pg. 1 lines 26-27.
[2] Office Action, pg. 3.
[3] Truex, col. 4 lines 38-40.
[4] Truex, FIG. 3.

Further, Applicant cannot find in the cited portions of these references, "wherein one I/O conductor provides an electrical connection to the constant voltage plane" as presently recited in claim 1. Applicant cannot find in the cited portions of Hittman a connection of a lead wire 12 to a constant voltage plane, or in the cited portions of Truex, a connection of a printed conductor 56 to a constant voltage plane.

The Office Action does not show where the feature is disclosed in Hittman and Truex, but instead rejects the feature under § 112 first paragraph.[5] However, as set forth above, the feature does indeed comply with the written description requirement. Therefore, Hittman with Truex does not teach or suggest all of the elements recited or incorporated into the claims.

Further still, one of ordinary skill would not reasonably be led to combine Hittman and Truex. Hittman states that "it is critical that the filtering take place as close as to the source of the emissions as possible, such as the entrance to the housing of the implantable device."[6] In Truex the filters are placed further away from the entrance to the housing (*see*, Truex FIG. 1) than in Hittman. Thus, Hittman teaches away from Truex. Also, Hittman refers to a filter feedthrough assembly having one or more lead wires 12 sealed with a hermetic seal insulator 20. The insulator 20 may be glass or ceramic material and is bonded to the lead wire 12 and ferrule 14 by brazed joints 24 and 26.[7] Truex states that such an assembly has problems resulting in loss of hermeticity.[8] Thus, Truex teaches away from Hittman. Because Truex teaches away from Hittman, and because Hittman teaches away from Truex, one of ordinary skill in the art would not be led to combine Hittman and Truex upon reading those documents.

The Office states that it would have been obvious to one of ordinary skill in the art ... to have a teaching of Truex employed in the apparatus of Hittman in order to reduce noise for the apparatus. However, Hittman refers to filtered feedthrough assemblies 100, 200 that provide protection from noise. Therefore, one of ordinary skill in the art would not reasonably be led to combine Truex with Hittman to solve a problem already solved in Hittman.

Consequently, claim 1 is not obvious in view of the cited portions of Hittman and Truex. Dependent claims 2-6, 8-12, 15-18, and 23-26 are believed to be patentable for at least the

[5] Office Action, pg. 7 and pg. 2.
[6] Hittman, col. 2 lines 50-53.
[7] Hittman, Abstract and col. 4 lines 46-56.
[8] Truex, col. 1 line 43 through col. 2 line 5.

reasons set forth above. Applicant respectfully requests reconsideration and allowance of claims 1-6, 8-12, 15-18, and 23-26.

2. Claims 19-22 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Hittman and Truex, and further in view of Brendel et al. (U.S. Patent No. 6,529,103, "Brendel").

Applicant respectfully traverses the rejection because the cited portions of Hittman, Truex and Brendel, either separately or in combination, do not disclose, teach, or suggest some of the elements recited or incorporated into the claims. For example, Applicant cannot find

> a printed circuit interconnect substrate residing on the hermetic side of the hermetic seal, wherein the printed circuit interconnect substrate includes a multi-layer circuit board comprising a buried signal layer between first and second conductive layers, wherein each conductive layer is electrically connected to a constant voltage to form a constant voltage plane, and wherein the multi-layer circuit board is arranged substantially parallel to the hermetic seal and normal to the I/O conductors,

which is incorporated into the claims from claim 1. Consequently, Applicant respectfully requests reconsideration and allowance of claims 19-22.

3. Claims 13-14 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Hittman and Truex, and further in view of Andresakis et al. (U.S. Patent No. 6,657,849, "Andresakis").

Applicant respectfully traverses the rejection because the cited portions of Hittman, Truex and Andresakis, either separately or in combination, or when combined with the reasoning of the Office Action, do not disclose, teach, or suggest some of the elements recited or incorporated into the claims. For example, Applicant cannot find

> a printed circuit interconnect substrate residing on the hermetic side of the hermetic seal, wherein the printed circuit interconnect substrate includes a multi-layer circuit board comprising a buried signal layer between first and second conductive layers, wherein each conductive layer is electrically connected to a constant voltage to form a constant voltage plane, and wherein the multi-layer circuit board is arranged substantially parallel to the hermetic seal and normal to the I/O conductors,

which is incorporated into the claims from claim 1. Consequently, Applicant respectfully requests reconsideration and allowance of claims 13-14.

4. Claim 7 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Hittman and Truex, and further in view of Chee (U.S. Patent No. 6,657,133).

Applicant respectfully traverses the rejection because the cited portions of Hittman, Truex, and Chee, either separately or in combination, or when combined with the reasoning of the Office Action, do not disclose, teach, or suggest some of the elements recited or incorporated into the claims. For example, Applicant cannot find

> a printed circuit interconnect substrate residing on the hermetic side of the hermetic seal, wherein the printed circuit interconnect substrate includes a multi-layer circuit board comprising a buried signal layer between first and second conductive layers, wherein each conductive layer is electrically connected to a constant voltage to form a constant voltage plane, and wherein the multi-layer circuit board is arranged substantially parallel to the hermetic seal and normal to the I/O conductors,

which is incorporated into claim 7 from claim 1. Applicant respectfully requests reconsideration and allowance of claim 7.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's representative at (612) 371-2172 to facilitate prosecution of this application.

If necessary, please charge any additional fees or deficiencies, or credit any overpayments to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being filed using the USPTO's electronic filing system EFS-Web, and is addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 6th day of July, 2009.

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